

FEATURES

Isolated high-side and low-side outputs

High side or low side relative to input: $\pm 700 V_{PEAK}$

High-side/low-side differential: $700 V_{PEAK}$

0.1 A peak output current

High frequency operation: 5 MHz maximum

High common-mode transient immunity: $>75 \text{ kV}/\mu\text{s}$

High temperature operation: 105°C

Wide body, 16-lead SOIC

UL1577 2500 V rms input-to-output withstand voltage

APPLICATIONS

Isolated IGBT/MOSFET gate drives

Plasma displays

Industrial inverters

Switching power supplies

GENERAL DESCRIPTION

The ADuM1233¹ is an isolated, half-bridge gate driver that employs the Analog Devices, Inc., *iCoupler*[®] technology to provide independent and isolated high-side and low-side outputs. Combining high speed CMOS and monolithic transformer technology, this isolation component provides outstanding performance characteristics superior to optocoupler-based solutions.

By avoiding the use of LEDs and photodiodes, this *iCoupler* gate drive device is able to provide precision timing characteristics not possible with optocouplers. Furthermore, the reliability and performance stability problems associated with optocoupler LEDs are avoided.

In comparison to gate drivers employing high voltage level translation methodologies, the ADuM1233 offers the benefit of true, galvanic isolation between the input and each output. Each output can be operated up to $\pm 700 V_{PEAK}$ relative to the input, thereby supporting low-side switching to negative voltages. The differential voltage between the high side and low side can be as high as $700 V_{PEAK}$.

As a result, the ADuM1233 provides reliable control over the switching characteristics of IGBT/MOSFET configurations over a wide range of positive or negative switching voltages.

¹ Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; 7,075,329; and other pending patents.

FUNCTIONAL BLOCK DIAGRAM

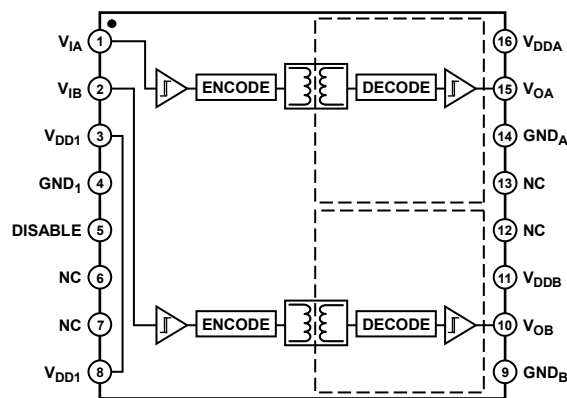


Figure 1.

Rev. B

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REVISION HISTORY

12/07—Rev. A to Rev. B

| | |
|-------------------------------------|---|
| Changes to Note 1..... | 1 |
| Change to Minimum Pulse Width | 3 |

4/07—Rev. Sp0: Rev. A

| | |
|----------------------------------|----|
| Changes to Figure 1 | 1 |
| Changes to Figure 7..... | 7 |
| Updated Outline Dimensions | 10 |

7/06—Revision Sp0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

All voltages are relative to their respective ground. $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$, $12\text{ V} \leq V_{DDA} \leq 18\text{ V}$, and $12\text{ V} \leq V_{DDB} \leq 18\text{ V}$. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = 5\text{ V}$, $V_{DDA} = 15\text{ V}$, and $V_{DDB} = 15\text{ V}$.

Table 1.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|--|-------------------------------|-------------------------------------|--------------------|-----|----------------------|---|
| DC SPECIFICATIONS | | | | | | |
| Input Supply Current (V_{DD1} Pins) | | | | | | |
| Quiescent | $I_{DD1(Q)}$ | | 3.0 | 4.2 | mA | |
| 10 Mbps | $I_{DD1(10)}$ | | 6.0 | 9.0 | mA | |
| Output Supply Current (V_{DDA} and V_{DDB} Pins) | | | | | | |
| Quiescent | $I_{DDA(Q)}, I_{DDB(Q)}$ | | 0.3 | 1.2 | mA | |
| 10 Mbps | $I_{DDA(10)}, I_{DDB(10)}$ | | 16 | 22 | mA | $C_L = 200\text{ pF}$ |
| Input Currents | $I_{IA}, I_{IB}, I_{DISABLE}$ | -10 | +0.01 | +10 | μA | $0 \leq V_{IA}, V_{IB}, V_{DISABLE} \leq V_{DD1}$ |
| Logic High Input Threshold | V_{IH} | 2.0 | | | V | |
| Logic Low Input Threshold | V_{IL} | | | 0.8 | V | |
| Logic High Output Voltages | V_{OAH}, V_{OBH} | $V_{DDA} - 0.1,$ $V_{DDB} - 0.1$ | V_{DDA}, V_{DDB} | | V | $I_{OA}, I_{OB} = -1\text{ mA}$ |
| Logic Low Output Voltages | V_{OAL}, V_{OBL} | | | 0.1 | V | $I_{OA}, I_{OB} = +1\text{ mA}$ |
| Output Short-Circuit Pulsed Current ¹ | $I_{OA(SC)}, I_{OB(SC)}$ | 100 | | | mA | |
| SWITCHING SPECIFICATIONS | | | | | | |
| Minimum Pulse Width ² | PW | | | 80 | ns | $C_L = 200\text{ pF}$ |
| Maximum Switching Frequency ³ | | 10 | | | Mbps | $C_L = 200\text{ pF}$ |
| Propagation Delay ⁴ | t_{PHL}, t_{PLH} | 97 | 124 | 160 | ns | $C_L = 200\text{ pF}$ |
| Change vs. Temperature | | | 100 | | ps/ $^\circ\text{C}$ | $C_L = 200\text{ pF}$ |
| Pulse Width Distortion, $ t_{PLH} - t_{PHL} $ | PWD | | | 8 | ns | $C_L = 200\text{ pF}$ |
| Channel-to-Channel Matching, Rising or Falling Edges ⁵ | | | | 5 | ns | $C_L = 200\text{ pF}$ |
| Channel-to-Channel Matching, Rising vs. Falling Edges ⁶ | | | | 13 | ns | $C_L = 200\text{ pF}$ |
| Part-to-Part Matching, Rising or Falling Edges ⁷ | | | | 55 | ns | $C_L = 200\text{ pF}$, input $t_R = 3\text{ ns}$ |
| Part-to-Part Matching, Rising vs. Falling Edges ⁸ | | | | 63 | ns | $C_L = 200\text{ pF}$, input $t_R = 3\text{ ns}$ |
| Output Rise/Fall Time (10% to 90%) | t_R/t_F | | | 25 | ns | $C_L = 200\text{ pF}$ |

¹ Short-circuit duration less than one second.

² The minimum pulse width is the shortest pulse width at which the specified timing parameters are guaranteed.

³ The maximum switching frequency is the maximum signal frequency at which the specified timing parameters are guaranteed.

⁴ t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{ix} signal to the 50% level of the falling edge of the V_{ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{ix} signal to the 50% level of the rising edge of the V_{ox} signal.

⁵ Channel-to-channel matching, rising or falling edges is the magnitude of the propagation delay difference between two channels of the same part when the inputs are either both rising or falling edges. The supply voltages and the loads on each channel are equal.

⁶ Channel-to-channel matching, rising vs. falling edges is the magnitude of the propagation delay difference between two channels of the same part when one input is a rising edge and the other input is a falling edge. The supply voltages and loads on each channel are equal.

⁷ Part-to-part matching, rising or falling edges is the magnitude of the propagation delay difference between the same channels of two different parts when the inputs are either both rising or falling edges. The supply voltages, temperatures, and loads of each part are equal.

⁸ Part-to-part matching, rising vs. falling edges is the magnitude of the propagation delay difference between the same channels of two different parts when one input is a rising edge and the other input is a falling edge. The supply voltages, temperatures, and loads of each part are equal.

ADuM1233

PACKAGE CHARACTERISTICS

Table 2.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|--|------------------|-----|------------------|-----|------|-----------------|
| Resistance (Input-to-Output) ¹ | R _{I-O} | | 10 ¹² | | Ω | f = 1 MHz |
| Capacitance (Input-to-Output) ¹ | C _{I-O} | | 2.0 | | pF | |
| Input Capacitance | C _I | | 4.0 | | pF | |
| IC Junction-to-Ambient Thermal Resistance | θ _{JA} | | 76 | | °C/W | |

¹ The device is considered a two-terminal device: Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.

REGULATORY INFORMATION

The ADuM1233 is approved by the organizations listed in Table 3.

Table 3.

| UL ¹ |
|---|
| Recognized under the UL1577 component recognition program |

¹ In accordance with UL1577, each ADuM1233 is proof tested by applying an insulation test voltage ≥ 3000 V rms for one second (current leakage detection limit = 5 μA).

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 4.

| Parameter | Symbol | Value | Unit | Conditions |
|--|--------|-----------|-------|--|
| Rated Dielectric Insulation Voltage | | 2500 | V rms | 1 minute duration |
| Minimum External Air Gap (Clearance) | L(I01) | 7.7 min | mm | Measured from input terminals to output terminals, shortest distance through air |
| Minimum External Tracking (Creepage) | L(I02) | 8.1 min | mm | Measured from input terminals to output terminals, shortest distance path along body |
| Minimum Internal Gap (Internal Clearance) | | 0.017 min | mm | Insulation distance through insulation |
| Tracking Resistance (Comparative Tracking Index) | CTI | >175 | V | DIN IEC 112/VDE 0303 Part 1 |
| Isolation Group | | IIIa | | Material Group (DIN VDE 0110, 1/89, Table 1) |

RECOMMENDED OPERATING CONDITIONS

Table 5.

| Parameter | Symbol | Min | Max | Unit |
|--|-------------------------------------|-----|------|-------|
| Operating Temperature | T _A | -40 | +105 | °C |
| Input Supply Voltage ¹ | V _{DD1} | 4.5 | 5.5 | V |
| Output Supply Voltages ¹ | V _{DDA} , V _{DDB} | 12 | 18 | V |
| Input Signal Rise and Fall Times | | | 100 | ns |
| Common-Mode Transient Immunity, Input-to-Output ² | | -75 | +75 | kV/μs |
| Common-Mode Transient Immunity, Between Outputs ² | | -75 | +75 | kV/μs |
| Transient Immunity, Supply Voltages ² | | -75 | +75 | kV/μs |

¹ All voltages are relative to their respective ground.

² See the Common-Mode Transient Immunity section for additional data.

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 6.

| Parameter | Rating |
|--|--------------------------------------|
| Storage Temperature (T_{ST}) | -55°C to +150°C |
| Ambient Operating Temperature (T_A) | -40°C to +105°C |
| Input Supply Voltage ¹ (V_{DD1}) | -0.5 V to +7.0 V |
| Output Supply Voltage ¹ (V_{DDA} , V_{DDB}) | -0.5 V to +27 V |
| Input Voltage ¹ (V_{IA} , V_{IB}) | -0.5 V to $V_{DD1} + 0.5$ V |
| Output Voltage ¹ | |
| V_{OA} | -0.5 V to $V_{DDA} + 0.5$ V |
| V_{OB} | -0.5 V to $V_{DDB} + 0.5$ V |
| Input-to-Output Voltage ² | -700 V_{PEAK} to +700 V_{PEAK} |
| Output Differential Voltage ³ | +700 V_{PEAK} |
| Output DC Current (I_{OA} , I_{OB}) | -20 mA to +20 mA |
| Common-Mode Transients ⁴ | -100 kV/ μ s to +100 kV/ μ s |

¹ All voltages are relative to their respective ground.

² Input-to-output voltage is defined as $GND_A - GND_1$ or $GND_B - GND_1$.

³ Output differential voltage is defined as $GND_A - GND_B$.

⁴ Refers to common-mode transients across any insulation barrier. Common-mode transients exceeding the Absolute Maximum Ratings may cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ADuM1233

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

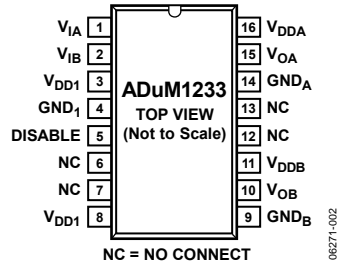


Figure 2. Pin Configuration

Table 7. ADuM1233 Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------------------------|------------------|--|
| 1 | V _{IA} | Logic Input A. |
| 2 | V _{IB} | Logic Input B. |
| 3, 8 ¹ | V _{DD1} | Input Supply Voltage, 4.5 V to 5.5 V. |
| 4 | GND ₁ | Ground Reference for Input Logic Signals. |
| 5 | DISABLE | Input Disable. Disables the isolator inputs and refresh circuits. Outputs take on default low state. |
| 6, 7, 12, 13 ² | NC | No Connect. |
| 9 | GND _B | Ground Reference for Output B. |
| 10 | V _{OB} | Output B. |
| 11 | V _{DDB} | Output B Supply Voltage, 12 V to 18 V. |
| 14 | GND _A | Ground Reference for Output A. |
| 15 | V _{OA} | Output A. |
| 16 | V _{DDA} | Output A Supply Voltage, 12 V to 18 V. |

¹ Pin 3 and Pin 8 are internally connected. Connecting both pins to V_{DD1} is recommended.

² Pin 12 and Pin 13 are floating and should be left unconnected.

Table 8. Truth Table (Positive Logic)

| V _{IA} /V _{IB} Input | V _{DD1} State | DISABLE | V _{OA} /V _{OB} Output | Notes |
|--|------------------------|---------|---|--|
| H | Powered | L | H | Output returns to input state within 1 μs of V _{DD1} power restoration. |
| L | Powered | L | L | |
| X | Unpowered | X | L | |
| X | Powered | H | L | |

TYPICAL PERFORMANCE CHARACTERISTICS

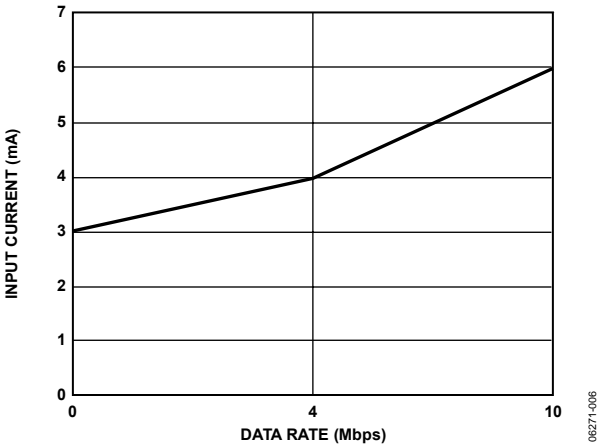


Figure 3. Typical Input Supply Current Variation with Data Rate

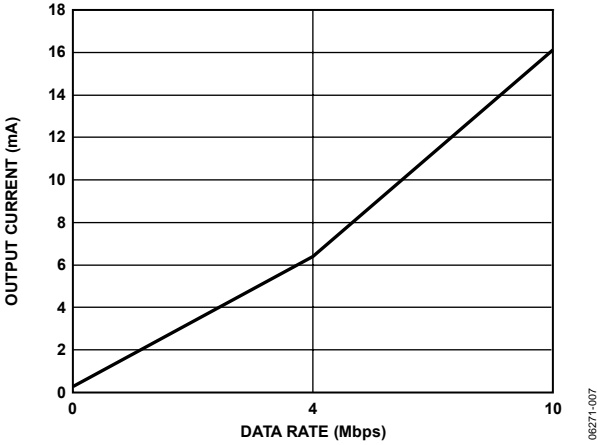


Figure 4. Typical Output Supply Current Variation with Data Rate

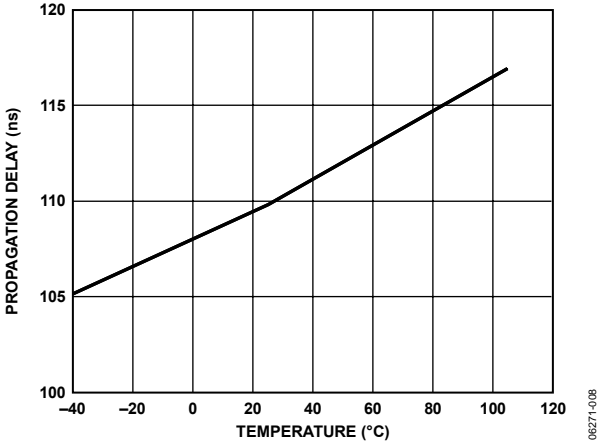


Figure 5. Typical Propagation Delay Variation with Temperature

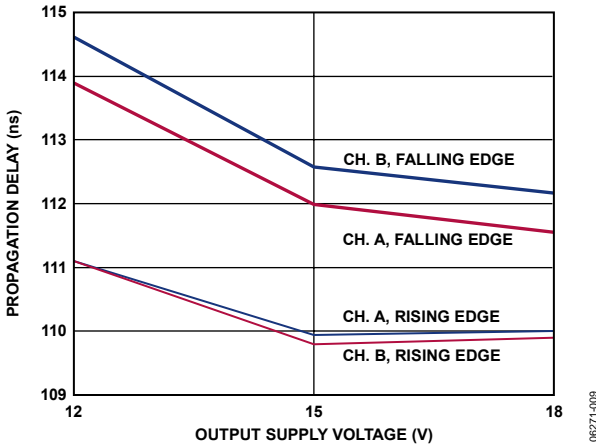


Figure 6. Typical Propagation Delay Variation with Output Supply Voltage (Input Supply Voltage = 5.0 V)

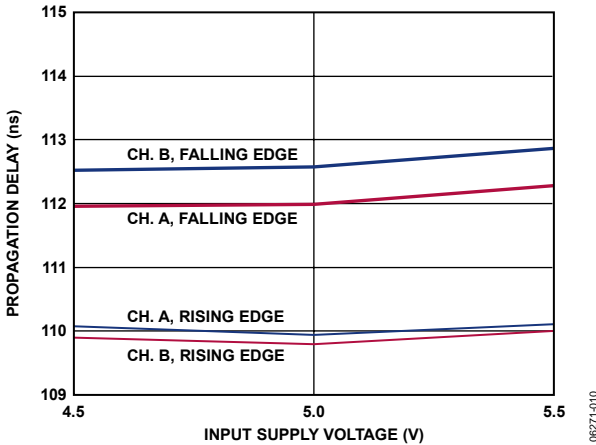


Figure 7. Typical Propagation Delay Variation with Input Supply Voltage (Output Supply Voltage = 15.0 V)

APPLICATIONS INFORMATION

COMMON-MODE TRANSIENT IMMUNITY

In general, common-mode transients consist of linear and sinusoidal components. The linear component of a common-mode transient is given by

$$V_{CM, linear} = (\Delta V / \Delta t) t$$

where $\Delta V / \Delta t$ is the slope of the transient shown in Figure 11 and Figure 12.

The transient of the linear component is given by

$$dV_{CM} / dt = \Delta V / \Delta t$$

The ability of the ADuM1233 to operate correctly in the presence of linear transients is characterized by the data in Figure 8. The data is based on design simulation and is the maximum linear transient magnitude that the ADuM1233 can tolerate without an operational error. This data shows a higher level of robustness than what is listed in Table 5 because the transient immunity values obtained in Table 5 use measured data and apply allowances for measurement error and margin.

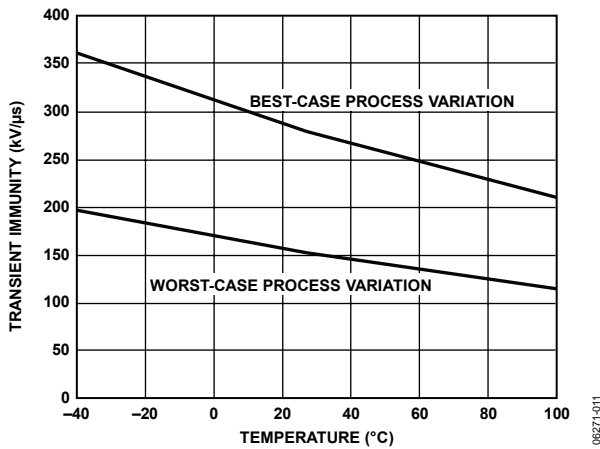


Figure 8. Transient Immunity (Linear Transients) vs. Temperature

The sinusoidal component (at a given frequency) is given by

$$V_{CM, sinusoidal} = V_0 \sin(2\pi ft)$$

where:

V_0 is the magnitude of the sinusoidal.

f is the frequency of the sinusoidal.

The transient magnitude of the sinusoidal component is given by

$$dV_{CM} / dt = 2\pi f V_0$$

The ability of the ADuM1233 to operate correctly in the presence of sinusoidal transients is characterized by the data in Figure 9 and Figure 10. The data is based on design simulation and is the maximum sinusoidal transient magnitude ($2\pi f V_0$) that the ADuM1233 can tolerate without an operational error. Values for immunity against sinusoidal transients are not included in Table 5 because measurements to obtain such values have not been possible.

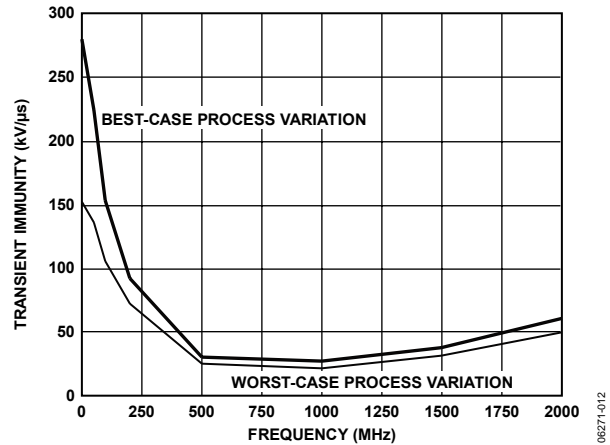


Figure 9. Transient Immunity (Sinusoidal Transients), 27°C Ambient Temperature

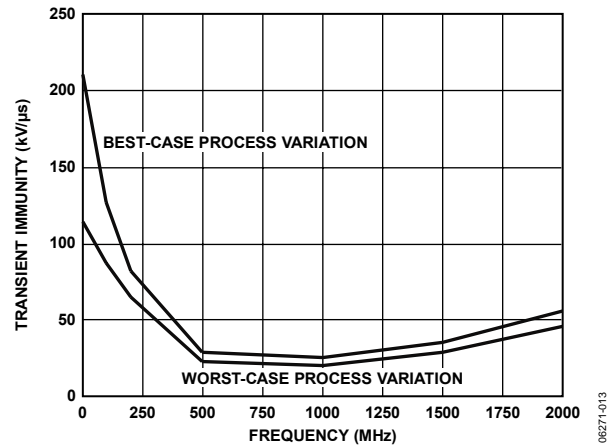


Figure 10. Transient Immunity (Sinusoidal Transients), 100°C Ambient Temperature

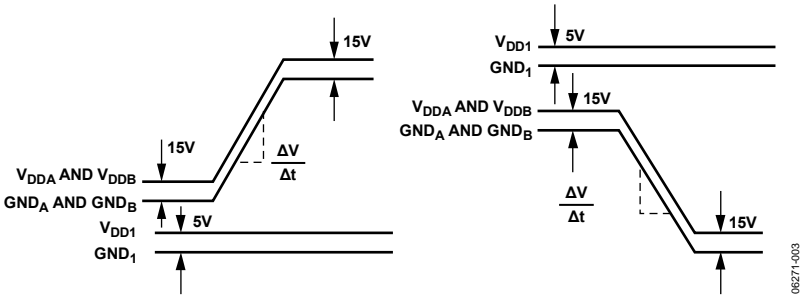


Figure 11. Common-Mode Transient Immunity Waveforms—Input to Output

06271-003

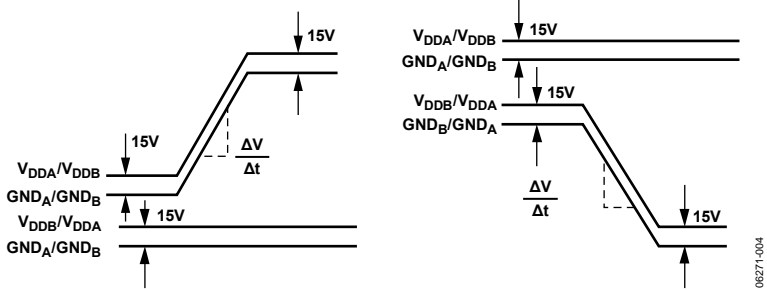


Figure 12. Common-Mode Transient Immunity Waveforms—Between Outputs

06271-004

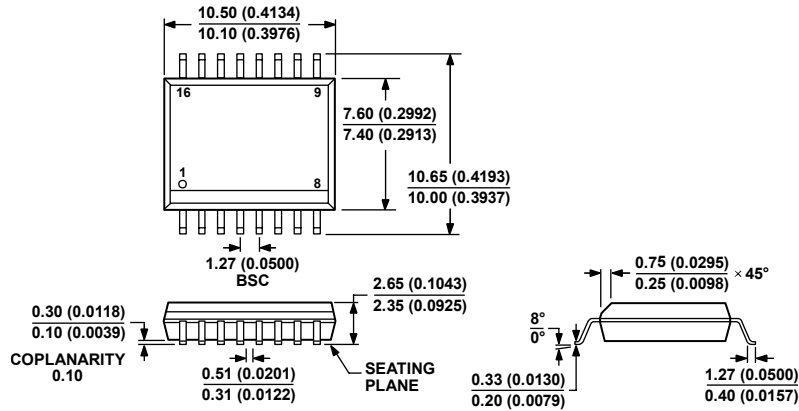


Figure 13. Transient Immunity Waveforms—Output Supplies

06271-005

ADuM1233

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 14. 16-Lead Standard Small Outline Package [SOIC_W]
 Wide Body (RW-16)
 Dimensions shown in millimeters and (inches)

032707-B

ORDERING GUIDE

| Model | No. of Channels | Output Peak Current (A) | Output Voltage (V) | Temperature Range | Package Description | Package Option |
|------------------------------|-----------------|-------------------------|--------------------|-------------------|--|----------------|
| ADuM1233BRWZ ¹ | 2 | 0.1 | 15 | -40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM1233BRWZ-RL ¹ | 2 | 0.1 | 15 | -40°C to +105°C | 16-Lead SOIC_W, 13-Inch Tape and Reel Option (1,000 Units) | RW-16 |

¹ Z = RoHS Compliant Part.

NOTES

ADuM1233

NOTES